REMARKS

This paper is being provided in response to the Office Action mailed June 27, 2005, for the above-referenced application. In this response, Applicants have cancelled claims 19 and 20 without prejudice or disclaimer of the subject matter thereof and amended claims 1, 4, 7 and 9 to clarify that which Applicants regard as the invention. Applicants respectfully submit that the amendments to the claims are fully supported by the originally-filed specification.

Applicants thank the Examiner for the indication of allowable subject matter in claims 3 and 7-18. Applicants have rewritten claims 7 and 9 into independent form to incorporate the features of the base claim and any intervening claims. Claims 8 and 10-18 depend therefrom. Accordingly, Applicants respectfully submit that these claims are in condition for allowance.

The objection to claim 1 for informalities has been addressed by amendments contained herein. Accordingly, Applicants respectfully request that this objection be reconsidered and withdrawn.

The rejection of claims 1, 2, 4-6, 19 and 20 under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,415,353 to Leung (hereinafter "Leung") is hereby traversed and reconsideration is respectfully requested in view of the amendments to the claims contained herein. Claims 19 and 20 have been cancelled herein.

Independent claim 1, as amended herein, recites a semiconductor memory device having a memory cell array comprised of memory cells requiring refresh, in which a read request or

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write request is asynchronously given for an access address. A refresh timer periodically outputs a refresh request signal for the memory cell array. A late write writing control circuit writes, for said write request, an access address and write data for a write request given in a memory cycle before a memory cycle for the write request by a late write operation. A refresh control circuit performs a refresh operation for said memory cell array in response to the refresh request signal from said refresh timer, and delaying performance of said refresh operation until a read operation or the late write operation for a memory cell for the read request or the write request is completed when said refresh request signal collides with said read request or said write request. The refresh control circuit includes circuitry that generates a control signal for said refresh operation and a control signal for the read operation or the late write operation based on (i) the refresh request signal and (ii) a delay signal responsive to the colliding of the read request or the write request with the refresh request signal. Claims 2 and 3 depend directly or indirectly from independent claim 1.

Independent claim 4, as amended herein, recites a semiconductor memory device having a memory cell array comprised of memory cells requiring refresh. A refresh request generator circuit generates a refresh request independently of a read request or write request for the memory cells. A refresh control circuit delays performance of the refresh until a read operation or write operation for said memory cells for said read request or write request is completed when the refresh request from said refresh request generator circuit collides with said read request or write request. The refresh control circuit includes circuitry that generates a control signal for said refresh operation and a control signal for the read operation or the write operation based on (i) said refresh request signal and (ii) a delay signal responsive to the colliding of the read

request or the write request with the refresh request signal. Claims 4-6 depend directly or indirectly from independent claim 4.

The Leung reference discloses a read/write buffer for complete hiding of the refresh of a semiconductor memory. A memory array requiring periodic refresh operations is controlled such that the refresh operations do not require explicit control signaling between the memory array and a memory controller. External accesses and refresh operations are handled such that refresh operations do not interfere with external accesses under any conditions. (See Abstract and col. 2, line 61 to col. 3, line 11 of Leung.)
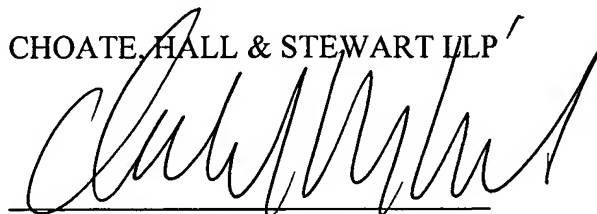
Applicants' independent claims 1 and 4, as amended herein, recite a semiconductor memory device including at least the features of a refresh control circuit that delays performance of the refresh operation until a read operation or write operation for a memory cell for the read request or the write request is completed when said refresh request signal collides with said read request or said write request, and wherein the refresh control circuit includes circuitry that generates a control signal for said refresh operation and a control signal for said read operation or said late write operation based on (i) said refresh request signal and (ii) a delay signal responsive to the colliding of said read request or said write request with said refresh request signal. Applicants have found that a semiconductor memory device that has the capability of delaying a refresh operation responsive to a collision of a refresh request with a read or write request helps the efficiency of and stabilizes the storage of the memory cells. (See, for example, page 35, line 3 to page 36, line 2 of the present application.)

Applicants respectfully submit that the Leung reference does not teach or fairly suggest at least the above-noted features as claimed by Applicants. Specifically, Leung discloses a semiconductor memory design in which read, write and refresh operations are *independently* controlled within each memory bank. (See col. 3, lines 2-8 of Leung.) Consequently, Applicants submit that Leung does not disclose a specific control relationship between read, write and refresh operations such as that claimed by Applicants. Leung system is selected to ensure that each of the memory banks is refreshed properly within a predetermined refresh period. (See col. 3, lines 28-31 of Leung.) Accordingly, Applicants submit that Leung does not disclose a refresh control circuit with circuitry that generates a control signal for said refresh operation and a control signal for said read operation or said late write operation based on (i) said refresh request signal and (ii) a delay signal responsive to the colliding of said read request or said write request with said refresh request signal, as is claimed by Applicants. Accordingly, Applicants respectfully request that this rejection be reconsidered and withdrawn.

Based on the above, Applicant respectfully requests that the Examiner reconsider and withdraw all outstanding rejections and objections. Favorable consideration and allowance are earnestly solicited. Should there be any questions after reviewing this paper, the Examiner is invited to contact the undersigned at 617-248-4038.

Respectfully submitted,

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